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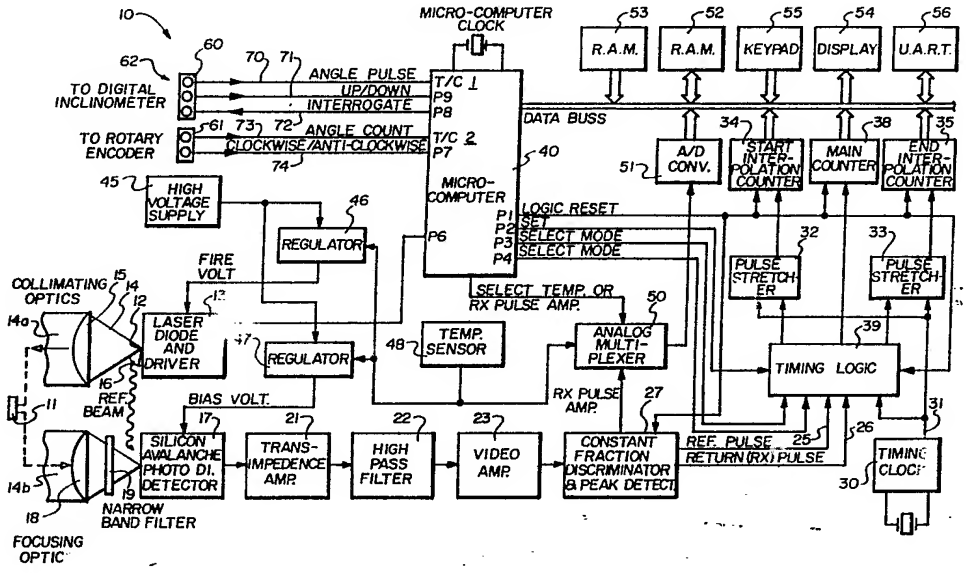

(57) Abstract

A laser detection system for determining distances and the rate of distance change with respect to a reference point (11) is disclosed. The system includes an infrared pulsing laser (13) in combination with infrared (IR) detector optics (18, 19) to detect (17) reflected (IR) pulses from a target. A timing device (39) is further included in the system to determine elapsed time between (IR) pulse generation and reflected pulse reception. A computer (40) controls laser operation and computes distance and rate of change of distance. The laser system may be used as a speed detector to determine the speed of a moving object or, in more rudimentary form, to measure distances from a reference point to an object or to measure one or more dimensions of an object.

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LASER DETECTOR SYSTEM

BRIEF DESCRIPTION OF THE INVENTION

Field of the Invention

This invention relates to measuring devices and is particularly concerned with measuring devices using LASER apparatus.

Prior Art

The need for devices that will measure distances and particularly that will measure the distance between fixed points and/or the distance between a fixed point and another movable point has long been recognized. Various geometrical instruments, such as transits, have been used in assisting the determination of such distances and other radar detectors and sonar detectors have also been used.

Radar detection units have become very popular and have long been used to determine the speed of traveling objects. Consequently, they are used for example by police departments to detect vehicle speeds and by others desiring to substantially instantly determine the speed of moving objects.

There have now also been developed a number of devices that will detect the presence of radar waves. Such devices are often used, for example, by motorists to warn them of the presence of radar waves sufficiently far in advance of detection by a police official that the motorist can reduce his speed to legal level, even though at the time the radar signal was detected the motorist may have been traveling at an illegal speed.

Because of the detectors now generally available, the use of radar detectors by the police does not provide as effective a vehicle speed deterrent system as is desired. Consequently, there is now a need for another speed detection system that will not be detected by the motorist, or even if detectable, that will provide

an alternative speed detection method that cannot be sensed by conventional radar detectors used by motorists.

Objects of the Invention

Principal objects of the present invention are to provide a distance measuring and speed detection system that is accurate, reliable and easily used in a portable form.

Other objects are to provide a detection system that will sense the speed of a moving object using sensed returned signal pulses that are not detectable with radar detection units and that are not easily detected other than by the signal generating and signal return receiving unit operated by a user.

Yet other objects are to provide a system of speed detection that uses a very short duration pulse of infrared light, generated, for example, by a semi-conductor laser diode and collimated into a narrow beam directed at a remote target.

Features of the Invention

Principal features of the invention include a semi-conductor laser diode as a short duration infrared light pulse generator; a light collimator; a silicon avalanche photodiode detector triggered as a timing reference; focusing optics to pick up a reflected light signal, to reflect it back to the photodiode detector; band filters; a transimpedance amplifier to transform the signal generated by the photodiode detector into a voltage; filters; boosters; a constant fraction discriminator and peak detector circuit; and a modified precision clock and a computer.

The system measures the velocity of a remote target by measuring the distance that the target travels

in a known time period. The distance to the target is determined by measuring the time of flight of a very short duration pulse of infrared light, generated by the semi-conductor laser diode. The greater portion of output of this diode is collimated in a narrow beam towards the remote target by the collimating optics. A smaller portion of the laser diode output is sent directly to the silicon avalanche photodiode detector (APD) in order to generate a timing reference. When the outgoing light pulse hits the distant target a small portion of the light that hits the target is reflected back to the instrument, where it is focused by the focusing optics onto the APD. Before the return pulse hits the APD it is filtered by a narrow band interference filter. This filter rejects all light except for a very narrow band around the wave length of the laser light. This improves the signal to noise ratio of the receiver and increases the range of the instrument. The signal current generated by the APD is transformed into a voltage by the transimpedance amplifier. It is then filtered by a high pass filter to reject any slowly varying interference signals. And finally boosted by a video amplifier and fed to the constant fraction discriminator and peak detector circuit. The peak detector circuit converts the analog signal into two digital timing pulses, i.e., a reference pulse and return pulse. The elapsed time between the rising edge of the reference pulse and the rising edge of the return or RX pulse from the target, is a direct measure of the time of flight of the pulse to the target and back. The peak detector circuit also generates a voltage output that is directly proportional to the amplitude of the RX pulse.

The elapsed time between the rising edge of the reference pulse and the rising edge of the RX pulse is determined by counting the number of cycles that occur from the precision clock. This clock is a crystal

controlled unit of high accuracy and high stability. Because the period of the timing clock offers too coarse a resolution for accurate operation of the instrument the fractional part of the clock period that the rising edge of the reference pulse occurs in and the fractional part of the clock period that the rising edge of the RX pulse occurs in must also be measured. This is accomplished by using two pulse stretchers to expand the time duration of these fractional portions so that two interpolation counters can acquire a count that relates to these fractional portions. The gating of the timing clock to a main counter and the operation of the pulse stretcher and interpolation counters are all controlled by the timing logic, which, in turn, is set up and controlled by the computer. The computer uses the count values in the main counter and the interpolation counters to determine the elapsed time between the rising edges of the reference and RX pulses to very high accuracy and resolution.

The elapsed time is then multiplied by the speed of light in air and divided by two to give the distance to the target. The division by two is necessary since the pulse travels twice the distance to the target, in going to and returning from the target. In order to calculate the velocity of the target the computer fires a number of pulses towards the target that are equally spaced in time. The resulting distances are stored in memory. The computer then calculates, using the method of least squares, the velocity of the target.

A high voltage source supplies two linear regulators. A regulator for the laser diode controls the fire voltage and a regulator for the APD controls the bias voltage. The fire voltage is adjusted so that the laser diode outputs the desired optical power. The bias voltage is adjusted so that the APD is operated at the desired sensitivity. Both linear regulators have a control input. These control inputs are led from a

temperature sensor that outputs a voltage that is proportional to the temperature of the instrument. So both the fire voltage and the APD bias voltage rise when the instrument temperature rises. This is necessary since the optical power output of the laser diode drops and the APD sensitivity falls with increasing temperature.

The output from the temperature sensor also feeds one input of an analog multiplexer, the other input is the RX pulse amplitude from the constant fraction discriminator circuit. On command from the computer either one of these two voltages can be fed to an analog to digital convertor (A/D) that digitizes these values so that the computer can read them. The computer uses these values to correct errors in the measured distance that arise from variations in temperature and RX pulse amplitude.

The computer, through its data base, communicates with the start and end interpolation counters; the main counter; an A/D converter; a random access memory (RAM); a read only memory (ROM); a display; a keypad; and a universal asynchronous receiver transmitter (UART). The computer program is contained in the ROM and the computer memory is the RAM. The keypad allows the operator to control the instrument functions and enter data accordingly. The display shows the distance or range to the target, the velocity of the target and other information items. The UART allows the instrument to communicate with external devices, such as other computers or data loggers.

The computer can also be interfaced to a digital inclinometer and a rotary encoder, via its timer/counter ports. So interfaced, the computer can read a vertical angle to the horizontal. This information will allow the computer, in conjunction with the range distance already acquired by the instrument, to

calculate the height of a remote object such as a tree, truck or the like. The rotary encoder in conjunction with a split image prism device allows the computer to determine the angle subtended in the horizontal plane by a remote object. Thus, the computer can also calculate the width of a remote object such as a tree, a power pole, vehicle, or the like.

The digital inclinometer generates a time pulse of width that is proportional to the inclination from the horizontal. It also generates a signal which tells the computer whether or not the tilt is up or down. There is also an interrogate line so that the computer can ask for this information on demand. The pulse that determines the inclination from horizontal goes to the timer/computer port 1 of the computer. Counter port 1 is set up as a timer so that the elapsed time of this pulse can be accurately determined relative to the computer clock. The computer clock is a highly accurate crystal controlled unit. The rotary encoder generates a series of pulses proportional to the angle through which the encoder is turned. The series of pulses is fed to the timer/counter port 2 of the computer, which is set up as a counter. The rotary encoder also generates a clockwise/anticlockwise signal and the two signals generated allow the computer to accurately calculate the shaft rotation of the rotary encoder and thus the width of a remote object target.

Other objects and features of the invention will become apparent from the following detailed description and drawings disclosing what are presently contemplated as being the best modes of the invention.

THE DRAWINGS

In the drawings:

Fig. 1 is a diagrammatic view of the overall laser detector system of the invention;

Fig. 2, a schematic diagram of the constant peak discriminator and peak detector;

Fig. 3, a schematic diagram of the pulse stretcher;

Fig. 4, a waveform diagram for the constant fraction discriminator and peak detector;

Fig. 5, a waveform diagram for the pulse stretcher;

Fig. 6, a timing logic diagram;

Fig. 7, timing logic waveform diagrams in TMAX/TMIN mode; and

Fig. 8, timing logic waveform diagrams in T LASER-mode.

DETAILED DESCRIPTION

Referring now to the drawings:

In the illustrated preferred embodiment, the Laser Detector system is shown generally at 10, in Fig. 1. As shown, a target 11, is the subject of the velocity determining components of the system. As shown, a short duration pulse of infrared light 12 is generated by a semi-conductor laser diode 13. The major portion 14 of the light is collimated into a narrow beam 14a by collimating optics 15. A smaller portion 16 of the light is sent directly to a silicon avalanche photodiode detector (APD) 17 to generate a timing reference, as will be further explained..

When the light pulse 14a hits the target 11 it is reflected back as reflected pulse 14b and is focused

through focusing optics 18 through a narrow band interference filter 19 onto the APD 17. The signal current generated by the APD is transformed into a voltage by the transimpedance amplifier 21. It is then filtered by a high pass filter 22 to reject any slowly varying interference signals. It is then boosted by a video amplifier 23 and fed to a constant fraction discriminator and peak detector circuit 24. The peak detector circuit converts the analog signal into two digital timing pulses, i.e., a reference pulse 25 and a return pulse 26. The peak detector circuit also generates a voltage output 27 that is directly proportional to the amplitude of the RX pulse.

A crystal controlled timing clock 30, of high accuracy and high stability generates a cyclic output 31 that measures the elapsed time between the rising edge of the reference pulse and the rising edge of the RX pulse. Because the period of the timing clock offers too coarse a resolution for accurate operation of the instrument the fractional part of the clock period that the rising edge of the reference pulse occurs in and the fractional part of the clock period that the rising edge of the RX pulse occurs in must also be measured. Thus, pulse stretchers 32 and 33 receive and expand the time duration of these fractional portions so that a start interpolation counter 34 and an end interpolation converter 35 can acquire a count that relates to these fractional portions. The gating of the timing clock to a main counter 38 and the operation of the pulse stretchers and interpolation counters are all controlled by the timing logic 39, which, in turn, is set up and controlled by a computer 40 The computer uses the count values in the main counter and the interpolation counters to determine the elapsed time between the rising edges of the reference and RX pulses to very high accuracy and resolution. The elapsed time is multiplied by the speed of light in air and

divided by two since the pulse travels twice the distance to the target to give the distance to the target. To calculate the velocity of the target the computer fires a number of pulses towards the target that are equally spaced in time. The resulting distances are stored in memory and the computer calculates the velocity of the target using the method of least squares.

A high voltage source 45 supplies two linear regulators 46 and 47. Regulator 46 controls the fire voltage of laser diode 13 and regulator 47 controls the bias voltage of the APD. The fire voltage is adjusted so that the laser diode outputs the desired optical power. The bias voltage is adjusted so that the APD is operated at the desired sensitivity. Each of the linear regulators 46 and 47 has a control input. The control inputs are fed from a temperature sensor 48 that outputs a voltage 49 that is proportional to the temperature of the instrument, whereby the fire voltage and the APD bias voltage rise when the instrument temperature rises as a means of compensating for less optical power output when the laser diode optical output drops and the APD sensitivity falls with increasing temperature.

The output from the temperature sensor 48 also feeds one input of an analog multiplexer 50, also having an input that is the RX pulse amplitude 27 from the constant fraction discriminator 24. On command from the computer 40 either one of these two voltages can be fed to an analog to digital converter (A/D) 51 that digitizes these values so that the computer 40 can read them. The computer uses these values to correct errors in the measured distance that arise from variations in temperature and RX pulse amplitude.

The computer, through its data base, communicates with the start and end interpolation counters 34 and 35; the main counter 38; the A/D converter 51; a random access memory (RAM) 52; a read

only memory (ROM) 53; a display 54; a keypad 55; and a universal asynchronous receiver transmitter (UART) 56.

The computer 40 is also interfaced to a digital inclinometer 60 and a rotary encoder 61, via its timer/counter ports. So interfaced, the computer 40 can read a vertical angle to the horizontal. This information will allow the computer, in conjunction with the range distance already acquired by the instrument, to calculate the height of a remote object such as a tree, terrain feature, power pole, vehicle, or the like. The rotary encoder in conjunction with a split image prism device 62 allows the computer to determine the angle subtended in the horizontal plane by a remote object. Thus, the computer can also calculate the width of a remote object such as a tree, a power pole, vehicle, or the like.

The digital inclinometer generates a time pulse 70 having a width that is proportional to the inclination from the horizontal. It also generates a signal 71 which tells the computer whether or not the tilt is up or down. There is also an interrogate line 72 so that the computer can ask for this information on demand. The pulse that determines the inclination from horizontal goes to the timer/counter port 1 of the computer. Counter port 1 is set up as a timer so that the elapsed time of this pulse can be accurately determined relative to the computer clock. The computer clock is a highly accurate crystal controlled unit. The rotary encoder generates a series of pulses 73 proportional to the angle through which the encoder is turned. The series of pulses is fed to the timer/counter port 2 of the computer, which is set up as a counter. The rotary encoder also generates a clockwise/anticlockwise signal 74 and the two signals allow the computer to accurately calculate the shaft rotation of the rotary encoder and thus the width of a remote object target.

The Constant Fraction Discriminator and Peak Detector Circuit 24 converts the analog reference 25 and RX pulses 26 into digital timing pulses. It also produces an output voltage that is proportional to the amplitude of the RX pulse. The circuit is shown in Fig. 2 and the associated wave forms are shown in Fig. 4. The operation of the circuit is as follows:

At the start of the measurement cycle when the logic reset line is held low flip flops 61 and 62 are both cleared so that the Q outputs are at logic zero, and similarly, the transmission gate T2 is closed during this time. This discharges capacitor C2 so that the output from voltage follower VF2 is zero. At this time there are no pulses from the video amplifier so the positive input to comparator CP1 is at zero. The negative input has a small positive offset voltage with respect to the positive input due to the bias voltage applied to resistor R3. This insures that the comparator output is in the low state. The value of the bias voltage is adjusted so that the comparator maintains its state in the presence of noise from the video amplifier 23. Transmission gate T1 is open at this time because the voltage on resistor R4 is zero. When the logic reset line is taken high, transmission gate T2 is open and the flip flops are ready to be clocked.

The reference pulse from the video amplifier 23 is sent to a delay line 63 which delays the pulse for a time (TD) while preserving the pulse shape. The output of the delay line feeds the positive input of the comparator CP1 and the voltage follower VF1 that drives the transmission gate T1. The reference pulse is also sent to a potential divider comprising resistors R1 and R2 which feeds the negative side of the comparator GP1. The values of R1 and R2 are chosen so that the reference pulse is divided by two when fed to the negative side. The delay time TD is set to approximately half the width

of the pulse at the fifty percent amplitude point. As seen in Fig. 4, the voltage on the positive input to the comparator exceeds the voltage on the negative input at approximately the fifty percent point on the rising edge of the pulse, causing the comparator output to change state. This switching point is substantially independent of the pulse amplitude and therefore is properly called a constant fraction discriminator. Because of the small offset voltage across the comparator inputs and the variation of the comparator response time with input overdrive the switching point shows small variations with changing pulse amplitude. A peak detector is used so that the computer knows the amplitude of the pulse and can apply an appropriate correction factor.

The output of comparator CP1 is sent to the timing logic 39 and to flip flops 61 and 62. When the reference pulse arrives the rising edge of the output of the comparator clocks flip flop 61 so that Q61 goes to a logic 1. Q62 stays at logic 0 since D was at logic 0 at the time of the clock pulse. Consequently, transmission gate T1 stays open for the duration of the reference pulse and the output from voltage follower VF2 remains at zero. When the RX pulse from the target arrives the same sequence of events occurs as for the reference pulse, except that the D input to flip flop 62 is now at logic 1. So when flip flop 62 is clocked on the rising edge of the comparator output the Q62 output goes to a logic 1. The Q62 output is differentiated by CP1 and resistor R4 and is sent to the transmission gate T1, so that the transmission gate closes for a short time. Since the timing of this gate closure is constant, in relation to the pulse, the voltage that capacitor C2 charges up to during the time the gate T1 is closed is proportional to the pulse amplitude. The output from voltage follower VF2 is a voltage whose value is proportional to the peak amplitude of the received pulse from the target.

The pulse stretcher takes an input pulse from the timing logic and generates an output pulse of longer duration. The variation of duration of the output pulse is exactly proportional to the variation of duration of the input pulse. The pulse stretcher circuit is shown in Fig. 3 and the corresponding wave forms in Fig. 5. The wave forms in Fig. 5 are not to scale and, in actuality, the pulse expansion is considerably larger than is shown in the diagram.

The input from the timing logic 39 controls current switch CS1. This switch steers the current I1, from the constant current source CC1, between either ground or the node containing the pulse stretch capacitor C3. At the start of the measurement cycle the input from the timing logic is at logic zero and current I1 is switched to the ground point. The current I2 into constant current sink CC2 discharges capacitor C3 until the diode D1 conducts and balances the current. The voltage of C3 at the start of the measurement cycle is the clamp voltage minus the voltage drop across D1. I1 is typically equal to one hundred times the value of I2, so that when the timing input goes high capacitor C3 is rapidly charged by the current difference (I1-I2). The voltage across capacitor C3 is buffered by the voltage follower VF3 and is fed to the positive input to comparator CP2. When the voltage on the positive input exceeds the reference voltage on the negative input the output from the comparator goes high. This allows timing pulses from the timing clock through to the interpolation counter since the output to the interpolation counter is the logical and of the output of comparator CP2 and the timing clock. When the input from the timing logic goes back to logic zero the current switch again changes over so that I1 is diverted to ground. Capacitor C3 now discharges at a much slower rate due to I2. When the voltage on capacitor C3 falls below the reference voltage

the comparator output drops back to logic zero. At this point in time the interpolation counter contains a count that relates to the width of the output pulse. Capacitor C3 continues to discharge until the initial conditions are again reached whereby D1 is conducting and balancing I2. The reference voltage is set so that the comparator threshold is at the fifty percent point on the charging path for the TMIN pulse. this gives maximum freedom from error effects due to ringing and non-linearity at the switching points. Fig. 5 shows expansion for the TMIN, TLASER, and TMAX pulses wherein TMIN is one clock cycle in duration, TMAX is two cycles and TLASER varies between one and two cycles.

Since the variation in duration of the output pulse is precisely proportional to the variation in duration of the input pulse, the interpolation counter value for TMAX minus the interpolation counter value for TMIN is a number that represents exactly one clock period of the main timing clock. Similarly, the interpolation counter value for TLASER minus the interpolation counter value for TMIN is a number that represents the fractional part of the clock cycle. Therefore, this number divided by the number that represents the complete clock cycle is the numeric fraction of the clock cycle. Inasmuch as this result is a ratio of two numbers, the exact value of the pulse expansion is not important. The procedure used eliminates any errors due to component tolerances or drift in the pulse stretcher circuit.

The timing logic 39 (Fig. 6) has two main functions. The first function is to gate the timing clock 30 so that the main counter 38 counts the number of complete cycles of the timing clock 30 that occur between the rising edges of the reference pulse 25 and the RX pulse 26. The second function is to generate the interpolation pulses that are to be expanded by the pulse stretchers. The timing logic also generates two

reference pulses TMAX and TMIN. TMIN has a duration equal to exactly one cycle of the timing clock and TMAX has a duration equal to exactly two cycles of the timing clock.

The timing logic is shown diagramatically in Fig. 6. Fig. 7 shows the logic wave forms for generating the reference timing pulses TMAX and TMIN and Fig. 8 shows the logic wave forms for generating the interpolation pulses TLASER for the start pulse and TLASER for the end pulse. The operation of the circuit is as follows:

At the start of the measurement cycle the logic reset line is taken low for at least four periods of the timing clock. This insures that all flip flops Q73-Q80 are in their initial state. In this state Q73 is at logic 0, Q74 is at logic 0, Q75 is at logic 1 and Q76 is at logic 1. Similarly Q77 is at logic 0, Q78 is at logic 0, Q79 is at logic 1, and Q80 is at logic 1.

The computer 40 then sets the select lines into the multiplexer MUX2 such that the TMIN signal is sent to both pulse stretchers 32 and 33. This results in both interpolation counters 34 and 35 having a count that relates to TMIN. The computer then sets the select lines to MUX2 so that the TMAX signal is sent to the pulse stretchers. This results in both interpolation counters having a count that relates to TMAX. These four count values are saved in memory. The computer then resets all flip flops back to their initial state and the select lines to MUX2 are set so that the TLASER signal is sent to the pulse stretchers. Next the laser diode 13 is fired for a distance measurement. This results in both interpolation counters 34 and 35 having a count that relates to the fractional part of the timing clock cycle. At this point the main counter 38 contains the number of whole timing clock cycles that occurred between the reference and RX pulses.

The generation of the TMAX and TMIN signals is identical for both the start pulse stretcher 32 and the end pulse stretcher 33. Consequently, only the timing for the start pulse stretcher is hereafter described. First the computer 40 takes the set line low causing Q73 to go to a logic 1. On the next rising edge of the timing clock Q74 goes to a logic 1. Simultaneously NOT Q74 goes to a logic 0. The D input to flip flop Q75 is now at logic 0 so on the next rising edge of TIMING CLOCK Q75 goes to logic 0. Similarly on the following rising edge of TIMING CLOCK, since the D input to flip flop 76 is at 0 Q76 will also drop to logic 0. The outputs Q74 and Q75 are logically anded so that the TMIN output is only high when Q74 and Q75 are high simultaneously. This is exactly one clock period, since the propagation delays are symmetrical for both the rising and falling edge of TMIN. Similarly the outputs Q74 and Q75 are logically anded to generate the timing signal TMAX. This is exactly two clock periods in duration because of the symmetrical propagation delays on the rising and falling edges.

At the start of the distance measurement the logic reset line is again held low for at least four clock cycles. On going high the flip flops are ready to be clocked and in their initial state. In this mode the set line is held high at all times and when the logic reset line is held low the main counter and both interpolation counters are cleared. On the rising edge of the reference pulse from the constant fraction discriminator flip flop 73 is clocked so that Q73 goes to a logic 1. The D input to flip flop 74 is now at logic 1 so that on the next rising edge of TIMING CLOCK Q74 goes to logic 1 and simultaneously NOT Q74 goes to logic 0. At this point the main count is enabled since the main counter 38 is the logical and of Q74, NOT Q78 and NOT TIMING CLOCK. Since NOT Q78 is at logic 1 and will be

until the RX pulse arrives the MAIN COUNT is now enabled so that on all subsequent falling edges of TIMING CLOCK 30 the main counter will be incremented. The use of NOT TIMING CLOCK rather than TIMING CLOCK to increment the main counter ensures that only complete clock periods between the reference pulse RX pulse are counted. The D input to flip flop 75 is now at zero so that on the next rising edge of TIMING CLOCK Q75 goes to logic 0. The interpolation timing pulse TLASER for the start pulse stretcher is the logical and of Q73 and Q75. This pulse will vary in duration between TMIN and TMAX depending on the exact timing of the rising edge of the reference pulse in relation to the timing clock. The D input to flip flop 77 is now at logic 1 so that on the arrival of the RX pulse from the discriminator flip flop 77 is clocked and Q77 goes to logic 1. The D input to flip flop 78 is now at logic 1 so that on the next rising edge of TIMING CLOCK Q78 goes to logic 1. Simultaneously NOT Q78 goes to logic 0 causing MAIN COUNT to be disabled. The D input to flip flop 9 is now at logic 0 so that on the following rising edge of TIMING CLOCK Q79 goes to logic 0. The interpolation timing pulse TLASER of the end pulse stretcher is the logical and of Q79 and Q77. As with the TLASER signal for the start pulse stretcher the duration of this signal will vary between TMIN and TMAX in this case depending on the exact timing of the rising edge of the RX pulse in relation to the timing clock.

The selected interpolation pulse width varies between 1 and 2 clock periods rather than between 0 and 1 since electronic circuits do not operate instantaneously and there would be nonlinearity as the interpolation pulse width approached zero. Also when the current switch in the pulse stretcher switches, considerable ringing and distortion occurs on the capacitor wave form. These noted effects would contribute significant errors

if the interpolation pulse width was varied between 0 and 1. However, by varying the pulse width between one and two clock periods the reference voltage to the pulse stretch comparator is set so that the switching point of the comparator is always in the linear portion of the charge and discharge period and clear of the ringing and distortion.

Although a preferred form of my invention has been herein disclosed, it is to be understood that the present disclosure is by way of example and that variations are possible without departing from the subject matter coming within the scope of the following claims, which subject matter I regard as my invention.

THE CLAIMS

I Claim:

1. A laser detector system comprising
a high voltage supply;
a laser diode and driver receiving fire voltage from the high voltage supply, and discharging infrared light pulses;
collimating c tics through which a major portion of each infrared light pulse is directed to a target;
focusing optics receiving reflected infrared light pulses from the target;
a silicon avalanche photo diode detector (APD) receiving reflected infrared light pulses from the focusing optics and generating and outputing a voltage signal;
means directing a smaller portion of each infrared light pulse discharged by the laser diode to the APD as a timing reference pulse;
a peak circuit detector receiving the voltage signal from the APD, and actuating a reference pulse and a return (RX) pulse;
a timing clock generating a cyclic output;
timing logic means including the cyclic output from the timing clock for measuring the elapsed time between the rising edge of the reference pulse and the rising edge of the RX pulse;
a video display; and
a computer for (a) controlling operation of the laser diode and driver, (b) for multiplying the elapsed time between the rising edge of the reference pulse and the RX pulse by the speed of light and divide the result by two to obtain the distance from the system to the target and

repeating (b) with at least one additional pulse generated by the laser diode and driver and received by the APD, and for outputing signal means to send video display.

2. A laser detector system as in Claim 1, wherein the means including the cyclic output from the cyclic clock for measuring the elapsed time between the rising edges of the reference pulse and the rising edge of the RX pulse includes

pulse stretchers to expand the fractional portions of the period of the timing clock connected to the computer; and

interpolation counters controlled by the timing logic means and connected to the computer, whereby data from the pulse stretchers and the interpolation is used by the computer in outputing the signal to the video display.

3. A laser detector system as in Claim 3, further including means to increase fire voltage and APD bias voltage proportionate to temperature increases of the system.

4. A laser detector system as in Claim 3, wherein the means to increase fire voltage and APD bias voltage includes

a linear regulator for the laser diode; and a linear regulator for the APD.

5. A laser detector as in Claim 1, further including means to interface the computer to a digital inclinometer.

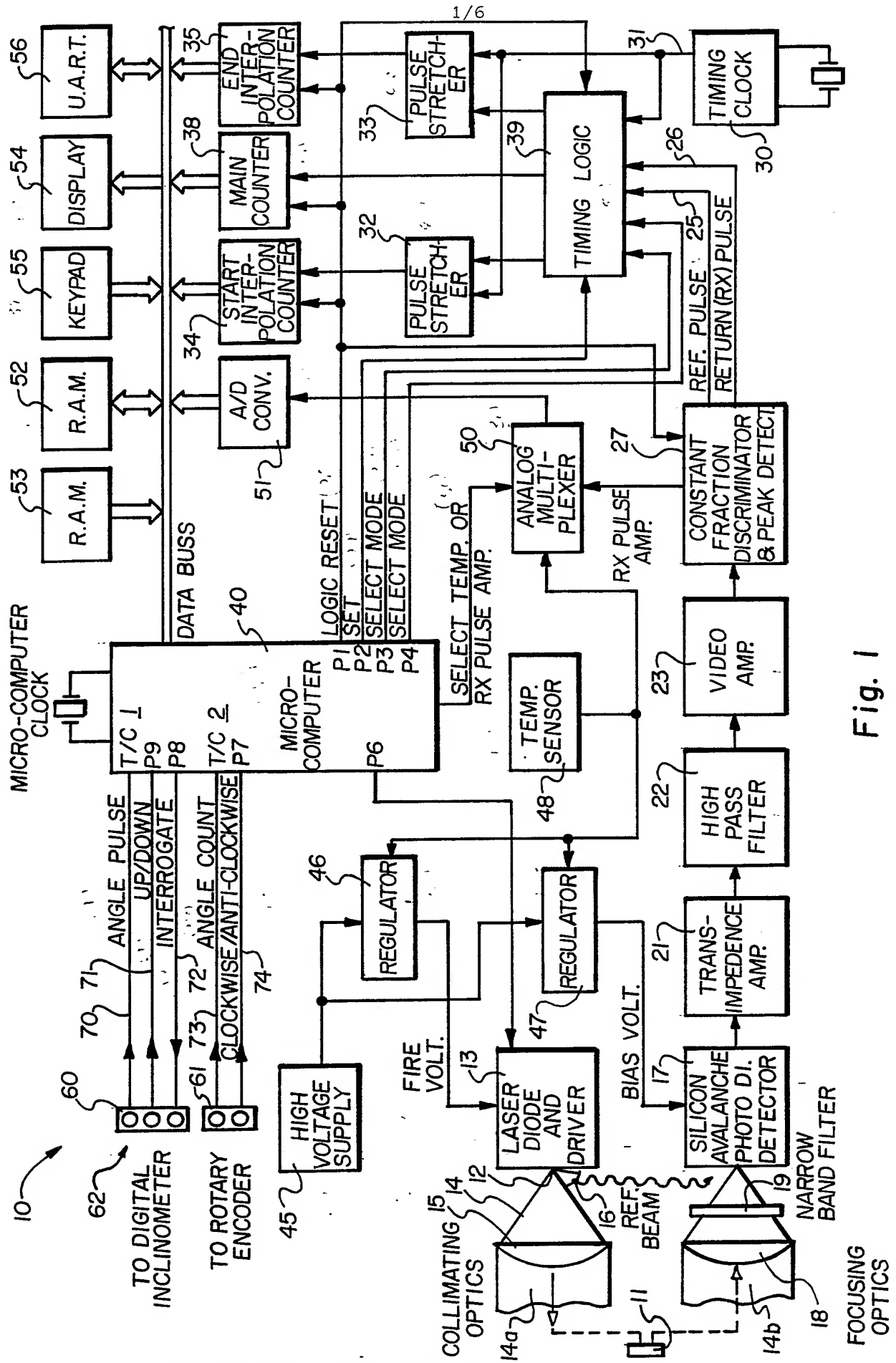
6. A laser detector as in Claim 1, further including means to interface the computer to a rotary encoder.

7. A laser detector as in Claim 5, further including means to interface the computer to a rotary encoder.

8. A laser detector as in Claim 1, further including means for varying the return (RX) pulse in response to sensed temperature variations.

9. A laser detector as in Claim 7, further including means for varying the return (RX) pulse in response to sensed temperature variations.

10. A laser detector as in Claim 8, wherein the means for varying the return (RX) pulse includes a temperature sensor that also provides an output to control fire voltage and APD bias voltage proportionate to temperature increases of the system.


MICRO-COMPUTER CLOCK
DATA BUSS
MICRO-COMPUTER
T/C 1
T/C 2
P1
P2
P3
P4
P6
P7
P8
P9
LOGIC RESET
SET
SELECT MODE
SELECT MODE
SELECT TEMP. OR RX PULSE AMP.
RX PULSE AMP.
REF. PULSE
RETURN (RX) PULSE
U.A.R.T.
DISPLAY
KEYPAD
R.A.M.
R.A.M.
R.A.M.
A/D CONV.
START INTER-POLATION COUNTER
MAIN COUNTER
END INTER-POLATION COUNTER
PULSE STRETCH-ER
PULSE STRETCH-ER
TIMING LOGIC
TIMING CLOCK
ANALOG MULTI-PLEXER
CONSTANT FRACTION DISCRIMINATOR & PEAK DETECT
TEMP. SENSOR
VIDEO AMP.
HIGH PASS FILTER
TRANS-IMPEDENCE AMP.
REGULATOR
REGULATOR
HIGH VOLTAGE SUPPLY
LASER DIODE AND DRIVER
SILICON AVALANCHE PHOTO DI. DETECTOR
NARROW BAND FILTER
FIRE VOLT.
BIAS VOLT.
ANGLE PULSE
UP/DOWN
INTERROGATE
ANGLE COUNT
CLOCKWISE/ANTI-CLOCKWISE
TO DIGITAL INCLINOMETER
TO ROTARY ENCODER
COLLIMATING OPTICS
REF. BEAM
FOCUSING OPTICS
10
11
12
13
14
14a
14b
15
16
17
18
19
21
22
23
25
26
27
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31
32
33
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56
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62
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71
72
73
74

Fig. 1

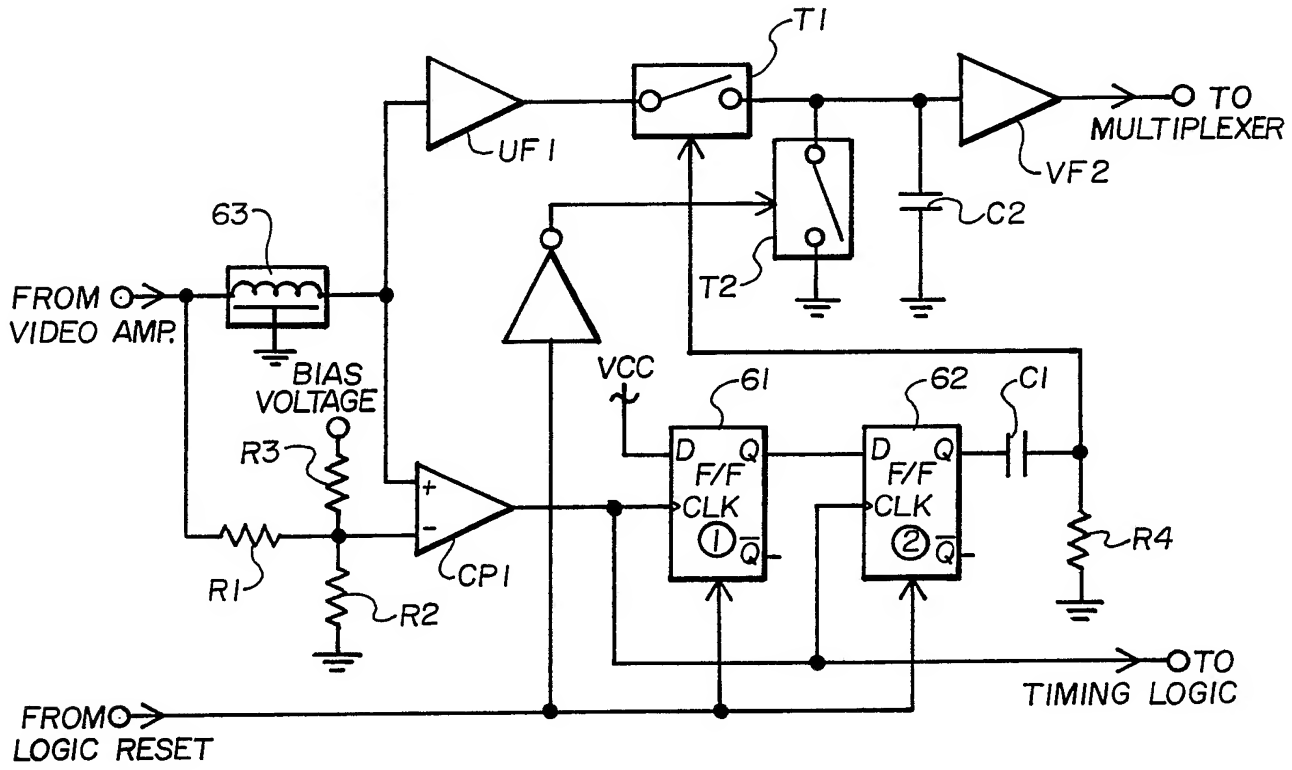
T1
UF1
TO
MULTIPLEXER
VF2
C2
63
T2
FROM
VIDEO AMP.
BIAS
VOLTAGE
VCC
61
62
C1
D
Q
F/F
CLK
R3
R4
R1
R2
CP1
TO
TIMING LOGIC
FROM
LOGIC RESET

Fig. 2

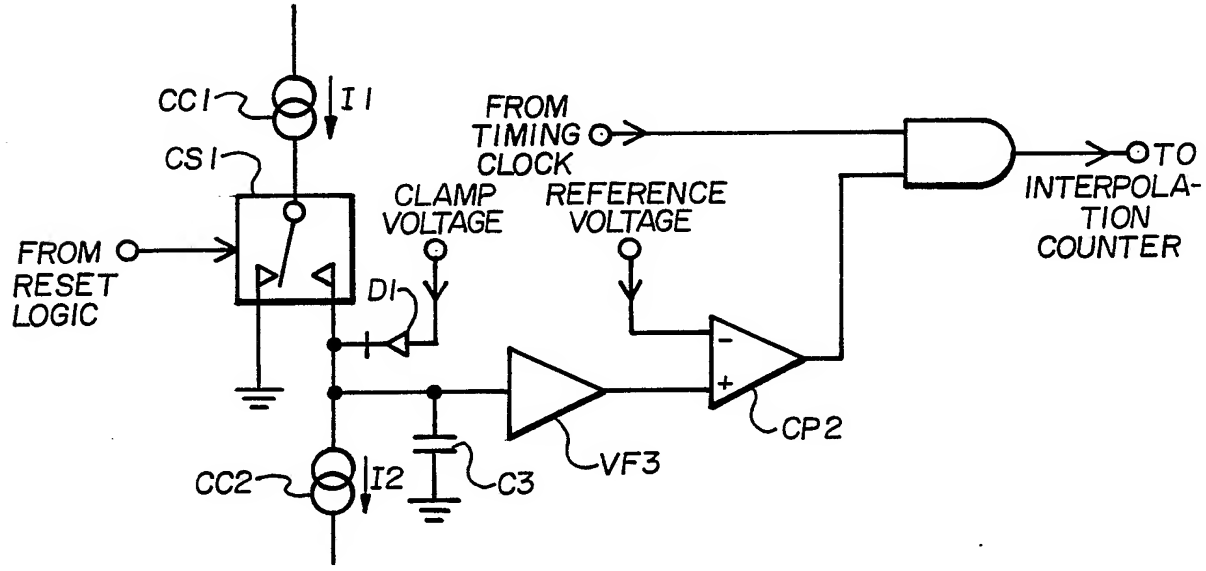
CC1
I1
CS1
FROM
TIMING
CLOCK
CLAMP
VOLTAGE
REFERENCE
VOLTAGE
TO
INTERPOLA-
TION
COUNTER
FROM
RESET
LOGIC
DI
CP2
VF3
CC2
I2
C3

Fig. 3

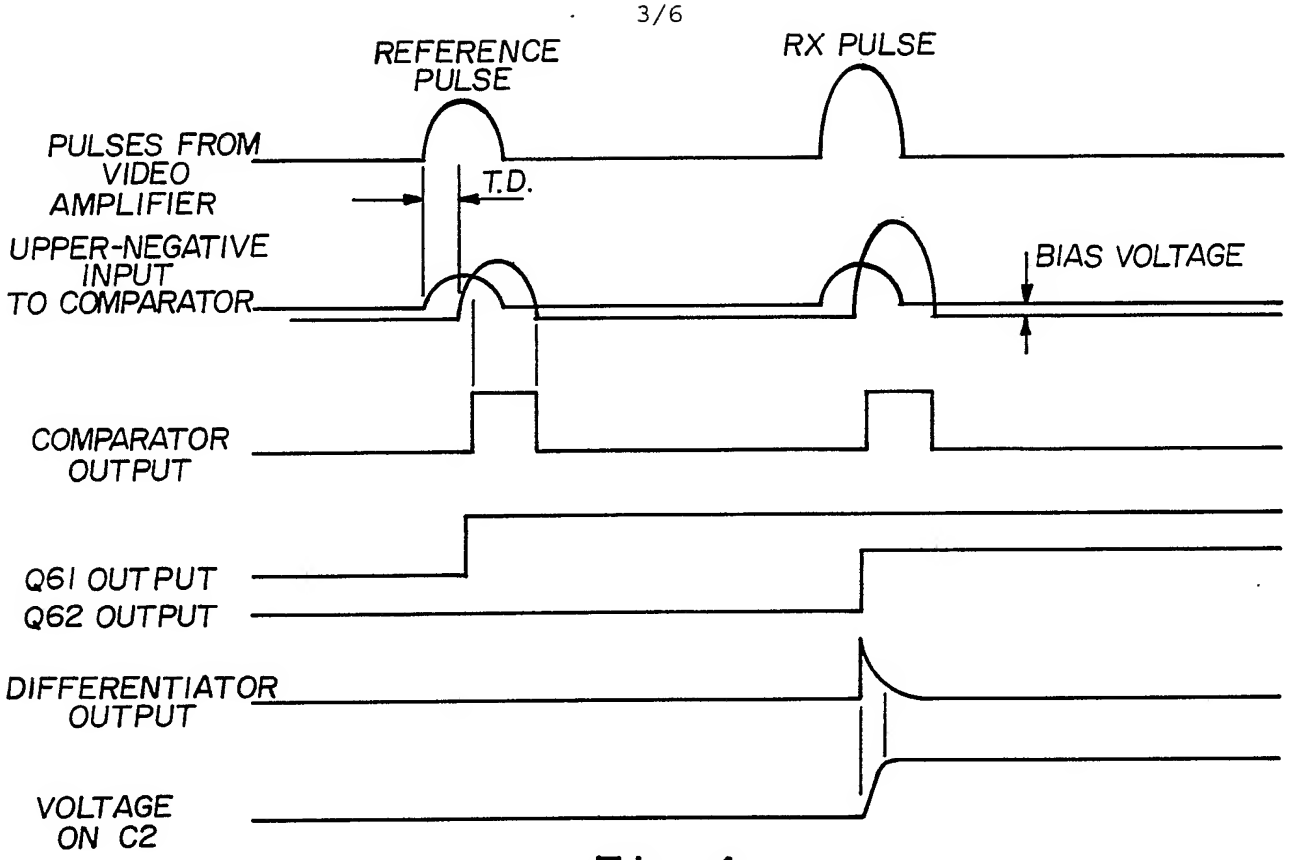
REFERENCE PULSE
RX PULSE
PULSES FROM VIDEO AMPLIFIER
T.D.
UPPER-NEGATIVE INPUT TO COMPARATOR
BIAS VOLTAGE
COMPARATOR OUTPUT
Q61 OUTPUT
Q62 OUTPUT
DIFFERENTIATOR OUTPUT
VOLTAGE ON C2

Fig. 4

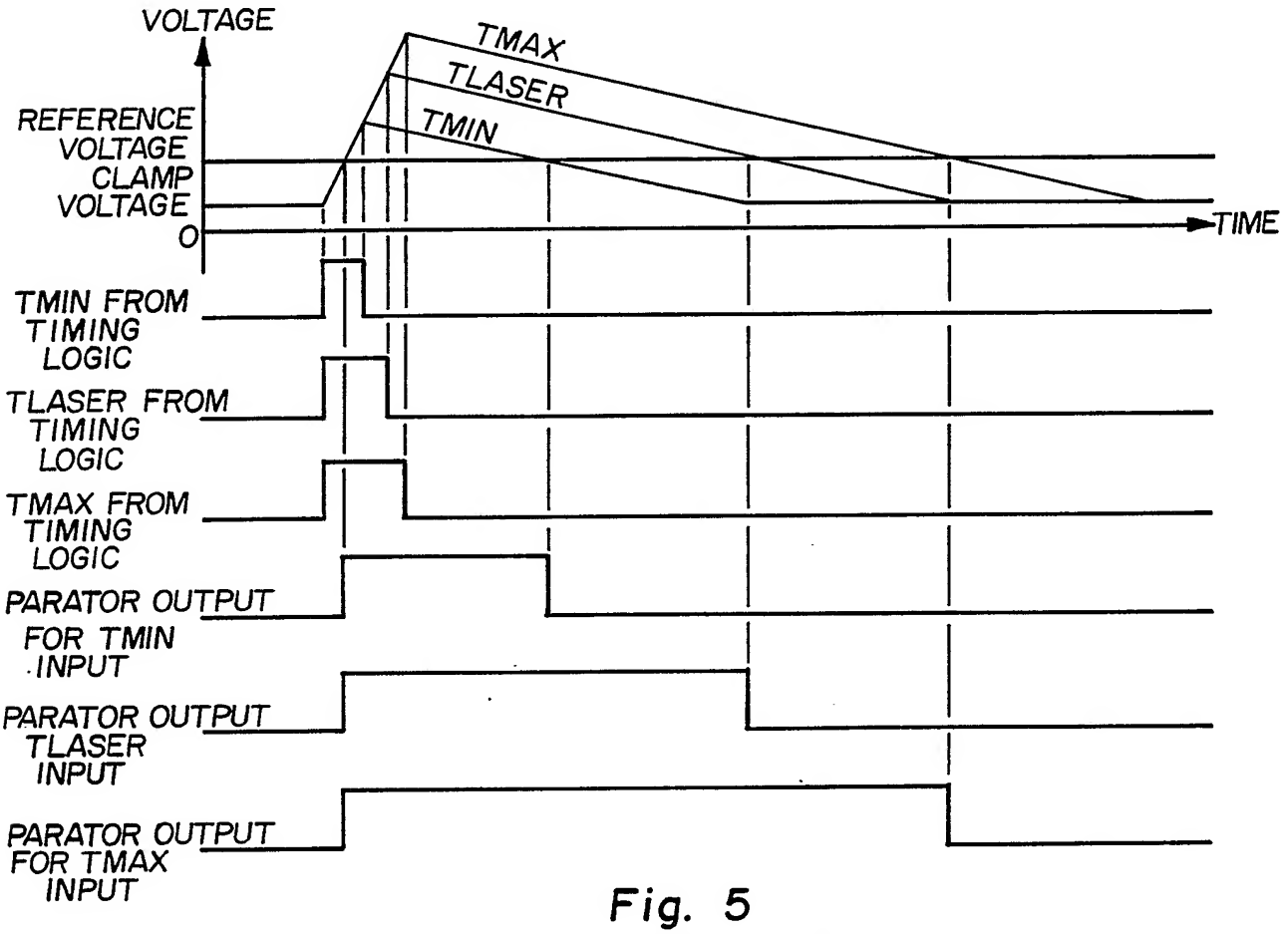
VOLTAGE
TMAX
TLASER
TMIN
REFERENCE VOLTAGE
CLAMP VOLTAGE
0
TIME
TMIN FROM TIMING LOGIC
TLASER FROM TIMING LOGIC
TMAX FROM TIMING LOGIC
PARATOR OUTPUT FOR TMIN INPUT
PARATOR OUTPUT TLASER INPUT
PARATOR OUTPUT FOR TMAX INPUT

Fig. 5

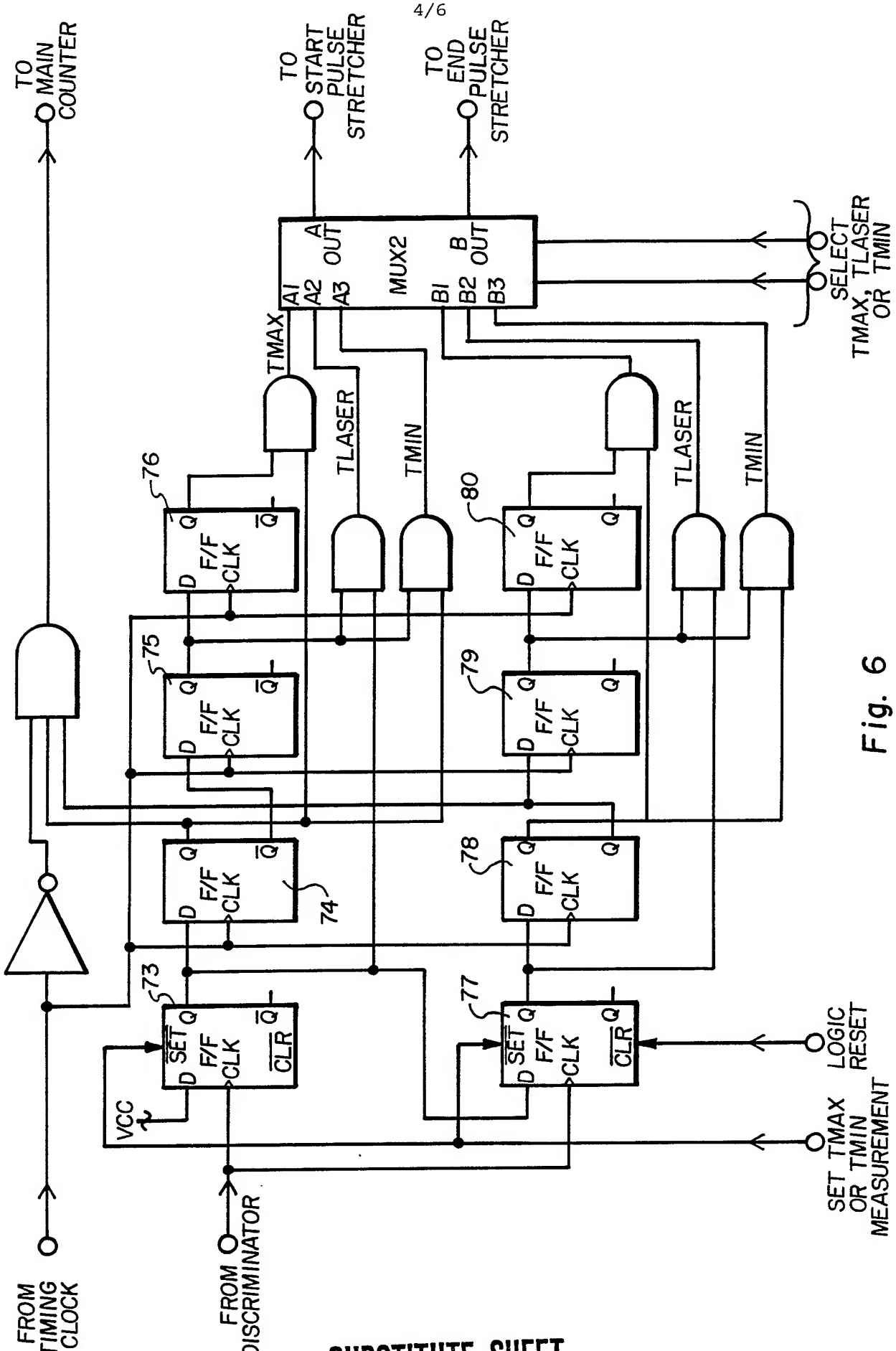
TO MAIN COUNTER
TO START PULSE STRETCHER
TO END PULSE STRETCHER
MUX2
A OUT
B OUT
A1 A2 A3
B1 B2 B3
SELECT TMAX, TLASER OR TMIN
TMAX
TLASER
TMIN
F/F
D
CLK
Q
SET
CLR
VCC
LOGIC RESET
SET TMAX OR TMIN MEASUREMENT
FROM TIMING CLOCK
FROM DISCRIMINATOR
73
74
75
76
77
78
79
80

Fig. 6

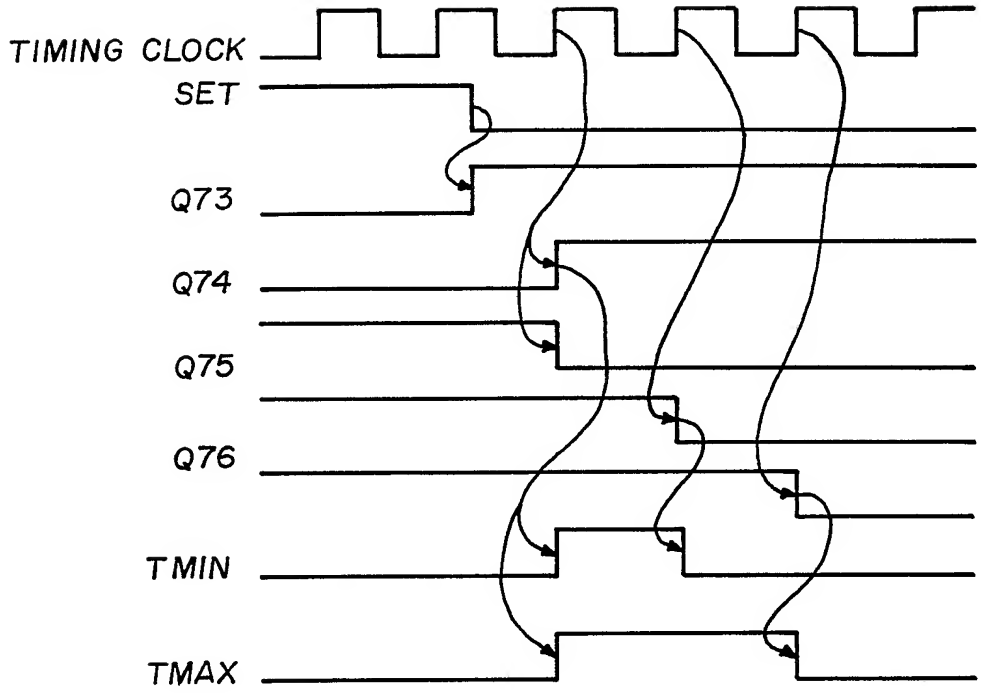

Fig. 7

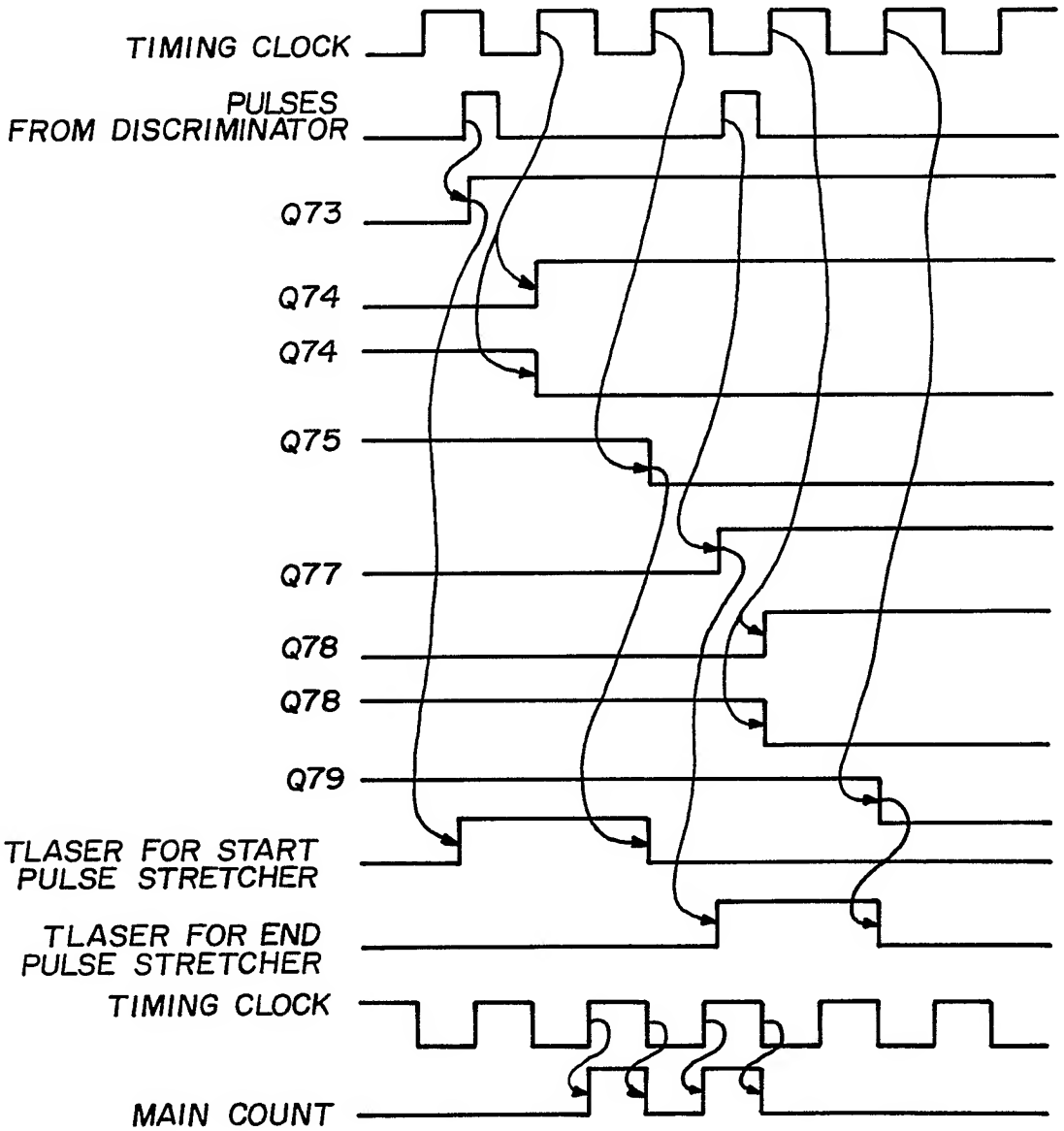
TIMING CLOCK
PULSES FROM DISCRIMINATOR
Q73
Q74
Q74
Q75
Q77
Q78
Q78
Q79
TLASER FOR START PULSE STRETCHER
TLASER FOR END PULSE STRETCHER
TIMING CLOCK
MAIN COUNT

Fig. 8

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/02293

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL. (5) G01C 3/08, 1/00; G01B 11/26
U.S. CL. 356/5,141

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	356/5,141

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4,734,587 (SCHWARTE) 29 March 1988	1-10
Y	US, A, 4,511,249 (FRUNGEL ET AL) 16 April 1985	1-10
Y	US, A, 4,113,381 (EPSTEIN) 12 September 1978	1-10
Y	US, A, 4,355,894 (MAEDA) 26 October 1982	3,8-10
Y	US, A, 4,722,599 (FRUENGEL ET AL) 02 February 1988	3,8-10
A	US, A, 4,770,526 (MANHART ET AL) 13 September 1988	1-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
20 JULY 1990	04FEB 1991
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	for STEPHEN C. BUCZINSKI

INTERNATIONAL DIVISION

Form PCT/ISA/210 (second sheet) (May 1986)